1.0 PURPOSE

This specification establishes the NEO Tech fabrication requirements for printed circuit boards. This specification applies to all Printed Circuit Boards procured by NEO Tech.

1.1 To provide NEO Tech suppliers with the standard quality and fabrication requirements unless otherwise noted.

1.2 To standardize NEO Tech requirements across the entire company.

2.0 SCOPE

Unless otherwise documented on purchase order or defined in documentation found in section, 3.0 ORDER OR PRECEDENCE, Printed Circuit Boards procured by NEO Tech will be in accordance with, Purchase Order Quality Clause (NEO-QU2001, latest revision) and PCB Fabrications specification (this document). This document supplements terms and conditions of the purchase order. If no document revision has been listed, the latest revision of all specifications shall apply. Any deviation to this specification, without written approval from NEO Tech are prohibited. Specific and approved deviation apply to a specific purchased part and does not constitute an amendment to the set forth specifications entirely.

3.0 ORDER OF PRECEDENCE

Principal flow down order of precedence, acceptance, fabrication and specification shall apply in the following order:

3.1 NEO Tech Purchase Order

3.2 Released Design Files and Fabrication Data / Drawing. This includes but not limited to, supporting procurement documentation, NEOTech and end customer engineering question, NEOTech Array Drawing, and text/readme files.

3.3 NEO Tech Customer Specifications

3.4 NEO Tech, PCB Fabrication Specification (this document)

3.5 All applicable IPC Standards

4.0 DEFINITIONS

Terms	Definitions
BUYER	NEO Tech companies and subsidiaries
SELLER	NEO Tech supplier
PO	Purchase Order
PCB	Printed Circuit Board
UL	Underwriter's Laboratories, Inc.
IPC	Association Connecting Electronics Industries

5.0 REFERENCE DOCUMENTS

The following documentation shall be the minimum referenced standard in the fabrications of NEOTech PCB Procurements.

Document #	Description
NEO-QU2001	Corporate Quality Clauses (Current revision)
IPC-A-600	Acceptability of Printed Boards
IPC-6011	Generic Performance Specification for Printed Boards
IPC-6012	Qualification and Performance Specification for Rigid Printed Boards
IPC-6013	Qualification and Performance Specification for Rigid-Flex and Flex Printed Circuit Boards
IPC-6016	Qualification and Performance Specification for High Density Interconnect (HDI) Layers and Boards
IPC-6018	Qualification and Performance Specification for High Frequency (Microwave) Printed Boards
IPC-4101	Laminate/Prepreg Materials Standards for Printed Boards
IPC-4552	Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards
IPC-4553	Specification for Immersion Silver Plating for Printed Circuit Boards
IPC-4554	Specification for Immersion Tin Plating for Printed Circuit Boards
IPC-SM-840	Qualification and Performance of Permanent Polymer Coating (Solder Mask) for Printed Boards
IPC-1601	Printed Board Handling and Storage Guidelines

Document #	Description
IPC-9252	Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards
IPC-2615	Printed Board Dimensions and Tolerance
IPC-TM-650	Test Methods Manual
J-STD-003	Solderability Test for Printed Boards
UL STD 94	Tests for Flammability of Plastic Materials for Parts in Devices and Appliances

6.0 ROLES AND RESPONSIBILITIES

6.1 SELLER (Supplier/Manufacture)

6.1.1 SELLER shall inform BUYER if there are any unresolved discrepancies between the BUYER purchase order, BUYER customer information and the BUYER specifications.

6.1.2 SELLER shall obtain latest revision and review all BUYER and CUSTOMER supporting documentation, fabrication information, applicable specifications, referenced on BUYER procurement documentation.

6.1.3 Design documentation provided by BUYER shall be considered confidential information and shall not be disclosed to third parties without BUYER prior written permission.

6.2 BUYER (NEOTech)

6.2.1 Corporate PCB Commodity Management shall maintain this document and assure that the BUYER website has the latest revision.

7.0 PROCEDURE AND FABRICATION REQUIREMENTS

Unless designated by BUYER (Section 3.0), all products are to be built to the following minimum standards; Procurement documentation and specifications, applicable IPC Qualification and Performance Specification (Section 5.0), Class 1,2 or 3 (latest revision), and the requirements in Section 7.0, whichever is more stringent. Any deviations to this specification, without written approval from BUYER, are strictly prohibited. Exceptions to this specification must be obtained in writing from BUYER on an individual part number basis.

7.1 Artwork and Fabrication Drawing Requirements

7.1.1 FABRICATION DATA for a first time purchase or new revision, BUYER shall provide to SELLER the most recent customer fabrication data which shall include at minimum Gerber files. If the customer data includes both ODB++ and Gerber data, and SELLER chooses to use the ODB++ data for fabrication, SELLER must compare the two data files. If there are discrepancies between the data files, it must be reported to BUYER and approval obtained before using the ODB++ data for fabrication. At no time shall SELLER use ODB++ format data for fabrication without comparing to Gerber format data.

7.1.2 Other than standard manufacturing allowances for produce ability, there shall be no modifications of the master artwork or Gerber data, or change in material specifications, without prior authorization from BUYER Engineering. All deviations to the fabrication drawing(s) or array drawing(s) must be approved by BUYER.

7.1.3 The SELLER is responsible for verifying that master artwork and/or Gerber data revision levels are in accordance with the master drawings and BUYER purchase order. If there are any discrepancies, BUYER shall be notified for resolution.

7.1.4 The fiducial diameter on the finished PCB must be within ± 0.002” of the original artwork/Gerber data.

7.1.5 All SELLER engineering questions on new PNs shall contain the stack-up for that Part Number. At a minimum, a stack-up shall show copper weights and thicknesses, material types, dielectric thicknesses, plies, types, of core/prepreg used and (Dk value, Impedance value and line width/space if applicable).

7.2 Array Requirements

7.2.1 X-outs (rejected pieces within the array) are not permitted unless indicated on BUYER procurement documentation, BUYER array drawing, or with written authorization from BUYER prior to shipment.

7.2.2 When X-outs boards are permitted, the following shall apply unless otherwise noted:

7.2.2.1 X-out boards must be identified by using a permanent black wide tip marker on both sides of the PCB or other identification method agreed to with BUYER engineering (in writing). The marking method used must withstand the entire assembly process and remain identifiable throughout.

7.2.2.2 The maximum # of X-outs per array is 10% or 1, whichever is greater. The maximum amount of X-out arrays per shipment is 10%. All X-outs boards must be packaged and labeled separately from the acceptable product.

7.2.2.3 X-out Panels may be use for solder sample.

7.3 Dimensional Requirements

7.3.1 Unless otherwise noted, tolerance .xx ± 0.01", .xxx ± 0.005".

7.3.2 Unless otherwise specified, board tooling hole locations to be ± 0.003" repeatable from board to board for automatic insertion. These tooling holes shall be drilled with the same program as the component holes. Tooling holes shall not be plated.

7.3.3 Bow and Twist must not exceed 0.75%. Measurement shall be in accordance with IPC-TM-650 2.4.22. Unless otherwise specified.

7.4 Edge Connector Requirements

7.4.1 Chamfered edge shall have no separation of plating and no loose metal or fibers on the beveled edge.

7.4.2 Unless otherwise specified, keying slots shall be centralized between printed connector contacts within BUYER's fabrication drawing tolerance.

7.5 Plating Requirements

7.5.1 All plating requirements to meet IPC-6012 OR IPC-6013 Class 2 or Class 3 (most current revision). Unless otherwise specified.

7.5.2 Plating thieving patterns are allowed within the borders of the BUYER array rails or frames, provided the plated area is copper and then covered with solder mask material. Plating thieving patterns shall be a minimum 0.200" from any fiducial or feature on the array. There shall be no plating thieving patterns within the area of the PCB without BUYER customer approval.

7.6 Wire Bond Pad Requirements

7.6.1 Bond Strength testing Per MIL-STD-883, Method 2011 (Destructive Bond Pull Test) or Method 2023 for (Non-Destructive Bond Pull Test). Condition shall be in accordance with the Customer Drawing.

7.6.2 PCB's that were rejected for anomalies that will not impact wire bond ability may be used for testing.

7.6.3 Pull Test Data and Coupons shall be included with each delivery.

7.7 Solder Mask Requirements

7.7.1 Solder masking must meet the acceptability requirements of IPC-SM-840 (Class 2 or Class 3) and IPC-A-600 (latest revisions) and be of the type specified on customer documentation.

7.7.2 No peeling, flaking, or blistering of the solder mask is allowed upon visual inspection or IPC tape testing (IPC Test Method IPC-TM-650 2.4.1).

7.7.3 Solder Mask shall withstand assembly and wash processes, and be compatible with all flux types (rosin based flux, no clean flux, and water soluble flux).

7.7.4 Via Plugging Height Shall be no greater than 0.003” above via pad.

7.7.5 Solder mask default is Green color (unless otherwise specified).

7.8 Silkscreen Requirements

7.8.1 Silkscreen shall be non-conductive and of contrasting color when not specified on procurement documentation. Silkscreen ink shall be cleared from solderable features.

7.8.2 Silkscreen default is White color (unless otherwise specified).

7.8.3 SELLER shall clip Silkscreen away from any exposed copper.

7.9 Electrical Testing

7.9.1 SELLER shall perform 100% Netlist Electrical verification (test) on all boards, using the data’s IPC-D-356 netlist. per IPC Specification 9252 (latest revision). Mark each board image to signify passing electrical tests.

7.9.2 Impedance Measurement Requirements: If an impedance requirement is identified on the drawing / specification, SELLER of the PCB shall perform impedance measurement of either PCBs or impedance coupons fabricated on the same working panels as the PCBs for each date code. Impedance coupons shall be traceable to the date code shipped.

7.9.3 HiPOT Test all Prepreg/Core material less than 0.1mm (4mil) thick at 500 VDC for 30 seconds minimum test should be done at the layer stage and prior packaging. *(If HiPOT test is required and specified in the fabrication drawing)*

7.10 Rework and Repair

7.10.1 Repairs or Welding traces is not allowed without written approval from BUYER.

7.10.2 Rework is permitted in accordance with applicable IPC standards as long as the rework does not result in damage or violate dimensional requirements.

7.10.3 Contact the BUYER to determine repair authority. Repair authority must be determined for each order prior to performing the repairs.

7.11 Markings

7.11.1 At minimum, SELLER to permanently mark date code with WWYY format, where WW is week and YY is year. Each board/array shall identify MANUFACTURER's U.L. code designation on each individual board that will remain legible through assembly and cleaning processes.

7.11.2 All boards, including boards fabricated in a multiple up array must be individually numbered, either in copper or silkscreen on the top side of the board.

7.12 Surface Finish Requirements

7.12.1 **Onshore SELLER Surface Finish Shelf Life: Im Ag**, **OSP, ISn, Electro-Tin** not be more than **five (5) months** and **ENIG** & all others **Surface finish** shall not be more than **ten (10) months** old per date code shall be submitted to BUYER for approval prior to shipment. Surface finish exceeding five or ten months shall be submitted to BUYER for approval prior to shipment. Submittal of solderability test data and solder float test data shall be included with submittal and prior to acceptance. BUYER written approval is required and test data shall be included with the shipment.

7.12.2 **Offshore SELLER Surface Finish Shelf Life: Im Ag**, **OSP, ISn, Electro-Tin** not be more than **three (3) months** and **ENIG** & all others **Surface finish** shall not be more than **eight (8) months** old per date code. Surface finish exceeding three or eight months shall be submitted to BUYER for approval prior to shipment. Submittal of solderability test data and solder float test data shall be included with submittal and prior to acceptance. BUYER written approval is required and test data shall be included with the shipment.

7.12.3 BUYER Facility Shelf Life Requirements

At Buyer Facility, when stored in the original packaging, surface finish shelf life requirements based on lot date code shall not exceed the following shelf life without BUYER engineering approval:

SURFACE FINISH:	Shelf Life
HASL (HOT AIR SOLDER LEVELING)	12 Months
LF-HASL (Lead-Free HASL)	12 Months
ENIG (ELECTROLESS NICKEL IMMERSION GOLD)	12 Months
ELECTROLYTIC **HARD GOLD** (GOLD & NICKEL THICKNESS TO BE SPECIFIED)	12 Months
BONDABLE SOFT GOLD (GOLD & NICKEL THICKNESS TO BE SPECIFIED)	12 Months
ENEPIG (NICKEL PALLADIUM)	12 Months
OSP (ORGANIC SOLDERABILITY PRESERVATIVE)	6 Months
ISn (IMMERSION TIN)	6 Months
Electro-Tin Plating	6 Months
Im Ag (IMMERSION SILVER)	6 Months

7.13 Quality Requirements

7.13.1 Board material must have a minimum rating of 94V-0 or the highest rating possible based on the laminate material type. The PCB fabrication process and materials shall be recognized by U.L., SELLER shall provide their U.L. File number on the Certificate of Conformance with each shipment.

7.13.2 Ionic Cleanliness, PCB's shall be measured prior to solder mask coating application in accordance with IPC-TM-650, Method 2.3.25, Resistance of Solvent Extract Method. The ionic contaminant level shall not be greater than 1.25 µg/cm^2 of sodium chloride.

7.13.3 Boards must meet the solderability requirements when tested in accordance with the J-STD-003 and appropriate Test Methods and Quality Clause **Solderability & Testing** (NEO-QU2001, latest revision). Results must be submitted for each date code supplied to BUYER along with the Certificate of Compliance. BUYER reserves the right to reject the entire date code of boards when samples cannot meet this criterion.

7.13.4 Plating thickness and hole wall integrity shall be verified in the smallest thru via and the smallest blind/buried via per Methods IPC-TM-650 2.1.1 for micro-section preparation and IPC-TM-650 2.6.8 for thermal stressing.

7.13.5 Board must be manufactured in accordance with the first article. No changes to the manufacturing location, chemistry, or material used in the deliverable PCB, including Subcontractors, shall be made without prior written authorization from BUYER.

8.0 DELIVERABLES AND SHIPPING DOCUMENTS *"The following deliverables and shipping documents are required with every delivery of fabrications in fulfillment of the purchase order":*

8.1 Certificate of Conformance: A Certificate of Conformance (CofC) is required with each shipment. Certificate of Conformance shall contain a statement certifying all requirement have been meet and any additional information invoked by subsequent Quality Clauses or this specification conform to the set forth specifications. Certificate of Conformance shall be signed by an authorized representative of the manufacturing organization. In conjunction with Quality Clause **First Article Inspection (FAI) Report** (NEO-QU1004, Latest revision) Certificate of Conformance shall include at a minimum:

- SELLER/Manufacturer Name
- NEO Tech Purchase Order #
- NEO Tech Part Number and revision
- Shipment Quantity
- Supplier Lot Code (work order #)
- Date Code
- Manufacturer UL File #

8.2 First Article Inspection Report: When applicable, the First Article inspection report shall be in accordance with Quality Clause **First Article Inspection (FAI) Report** (NEO-QU2001, latest revision).

8.3 Microsection Report: Microsection report shall include measurements in accordance with the applicable specification and IPC standards.

8.3.1 Micro-section potted coupon/s from report and the PCB it was taken from shall be included with the shipment.

8.4 Electrical Test Report: Report shall demonstrate 100% Electrical Testing, quantity tested, quantity pass, and test parameters in accordance with IPC-9252.

8.4.1 **Impedance Measurement Data:** When Impedance Measurement is required, Impedance test data shall be provided with each lot.

8.5 Solderability Data: Solderability results in accordance with Quality Clause **Solderability & Testing** (NEO-QU2001, latest revision) must be submitted for each date code supplied to BUYER along with the Certificate of Compliance.

8.6 Ionic Cleanliness Data: Ionic contamination report shall be included with each shipment and demonstrate conformance to procurement documentation.

8.7 Solder Sample: SELLER shall provide a bare, unsoldered sample PCB array for Solderability and thermal profile with each date code of parts shipped. Solder Sample may be a scrap array and not electrically functional. Sample shall be clearly marked and identified as a Solder Sample.

8.8 REACH/RoHS: When PCB procurement is specified on procurement documentation as REACH or RoHS compliant, a statement of compliance shall be provided.

8.9 Manufacturing Origin: All PCB procurements, including Brokers, Intermediate Organizations, Manufacturers Reps or Agents shall provide the manufacturer's name and facility location on the Certificate of Conformance with each shipment to BUYER

8.10 Additional Deliverables and documentation, not included in the above paragraphs, shall be identified via the purchase order notes.

9.0 PACKAGING REQUIREMENTS

9.1 Shipping boxes not to exceed 16 Kilogram (35 Pounds).

9.2 Shipping carton to be marked with SELLER name, date codes, vendor lot number, purchase order number, quantity in the carton, part number and revision number or per Bar Code Standards requested. If more than one date code is to be shipped in a box, they must be clearly identified on the packages.

9.3 All PCB shall be dry, cleaned and free of debris prior to packaging. In conjunction with Quality Clause **Packaging Requirements** (NEO-QU2001, latest revision), the packaging shall be done in a way to prevent damage to the

product edges / corners using industry acceptable methods (Reference IPC Spec 1601) and must include the following:

- Vacuum Sealed Moisture Barrier Packaging
- Humidity Indicator Card (HIC)
- Desiccant compatible with PCB and Surface Finish
- Slip sheets between each PCB
- Suitable bubble wrap

9.4 Solder Samples and cross section samples should be packaged separately at the top of the box.

9.5 X-outs, when permitted, shall be packaged separately from no X-out arrays and clearly marked.

9.6 When multiple separate packages are delivered as part of a shipment or an order fulfillment of a single fab PN, each bag shall contain single lot date code and be clearly marked/labeled with the following content information.

- Part Number
- PO Number
- Quantity per bag/container
- Date code(s) in bag/container

9.7 All Immersion Silver finish PCBs must be packed with silver saver paper in between each PCB.

10.0 Revision History (EtQ will automatically list the revision here)

Revision	Reason for Change	Effective Date
A	Update document to new document number.	Oct 7, 2020
B	7.12.3 Solderability & Testing to be NEO-QU2001 instead NEO-QU1004	Mar 31, 2021
C	7.11 Surface Finish Shelf Life updates 9.1 Shipping boxes weight update	March 7, 2024
D	7.6 Wire Bond Pads 7.9.3 Repair authority must be requested	February 1, 2026