Aluminum Nitride (Multilayer)
Design Guidelines

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Introduction

ALN Ceramic Technology

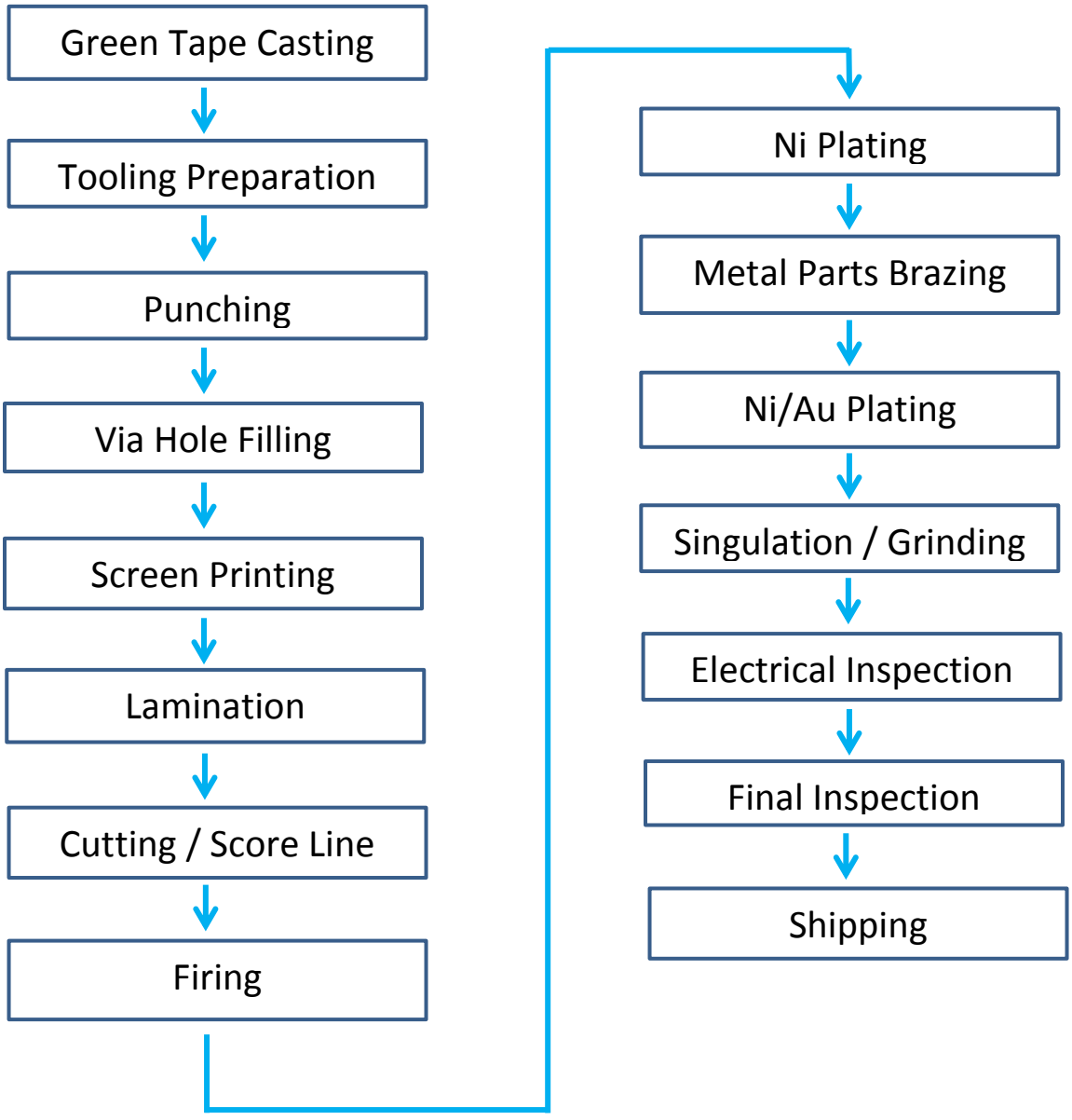
- Natel has been providing LTCC and AlN packaging solutions to microelectronics industry for over ten years. ALN Technology has evolved to incorporate embedded filters and more complex mechanical features.

- Natel has developed a vertically integrated AlN production process with internal controls on raw materials, tape casting, green processing, firing, and brazing.

- Natel's experience in ceramics processing that includes thick film, LTCC, AlN, and HTCC has resulted in the development of world's most reliable multilayer ceramics technology available to the microelectronics industry.

- Natel AlN technology allows tight dimensional controls along with 0.004" vias, line widths, and spacing. In addition to conventional multilayer technologies, Natel's current capabilities are presented in this design guide.

Basic Process Steps



Material Characteristics

Aluminum Nitride

Color	**Tan**
Bulk Density (gm/cc)	3.26
Dielectric constant 1 MHz 12. 5 GHz (measured by split cavity method)	 9.0 8.5
Dissipation Factor at 12.5 GHz (1×10^{-3})	2.38
Dielectric Strength (V/m)	1×10^{9}
Volume Resistivity (25 C) (Ω-cm)	10^{14}
Coefficient of Thermal Expansion (25 to 400 C)	4.44×10^{-6}
Thermal Conductivity (W/mK)	180±20
Modulus of Rupture (MPa)	300

Material Characteristics

Material options for I/O pins (lead frame), heat sinks, and seal rings when brazed to HTCC

Material	TCE ($X 10^{-6}$ / °C RT to 400 °C)	Thermal Conductivity (W/m ^{0}K	Specific Heat (J/Kg ^{0}K)	Density (g/cc)
Cu-Mo (85 Mo 15 Cu)	7.0	150	276	10
Cu-Mo-Cu (13-74-13)	5.6	>380	>200 in pane >170 thru plane	9.88
CuW	6.0	180	163	17.0
Cu	17	398	377	9.0
Kovar	5.5	17	460	8.4
AIN	4.4	170	670	3.3
Al-Si-C	6.9-8	>150	741-808	3.0

Conductor

Tungsten

Conductor Property	Surface (with Ni-Au plating)	Internal
Sheet Resistance	6 mΩ / sq. nominal 8 mΩ / sq. max.	10 mΩ / sq. nominal 15 mΩ / sq. max.
Via Resistance 0.008" Dia – 0.010" thick		< 4 mΩ
Insulation Resistance	≥1 X 10^{10} Ω	≥1 X 10^{10} Ω
Temperature Coefficient of Resistance (TCR)	4500 ppm/^{o} C	4500 ppm/^{o} C

Material Characteristics

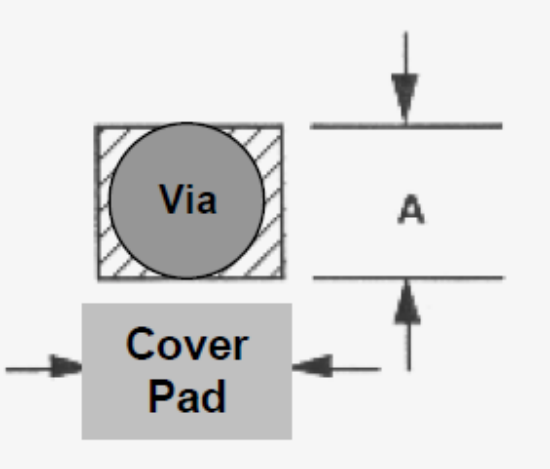
Ceramic Tape Standards

Description	Process	Comment
Layer Thickness	Green 0.0065 Fired 0.005 Green 0.013 Fired 0.010	Tape layer thickness may be custom designed between 0.002” to 0.020”
Layer Count	Up to 50 layers	
Fired X-Y shrinkage control	±0.3%	Natel provides best X-Y shrinkage control in the industry
Fired Thickness Control	±0.5%	
Flatness Control (as fired)	0.002 inch / inch	

Via Design Rules

Electrical Vias

Electrical via sizes for standard tape thicknesses (see table below). A maximum of three via diameters on any tape is offered as standard processing. Other via sizes and size quantities per layer is available upon request.



Tape Thickness*	**2 mil**	**5 mil**	**7.5 mil**	**10 mil**	**12 mils*** **	**15 mils*** **
Via dia A**	4,6,8,10 mils	4,6,8,10 mils	4,6,8,10 mils	4,6,8,10 mils	6,8,10 mils	8,10 mils

*Approximate fired thickness
** As punched unfired diameter
*** For prototype work only.

Via Design Rules

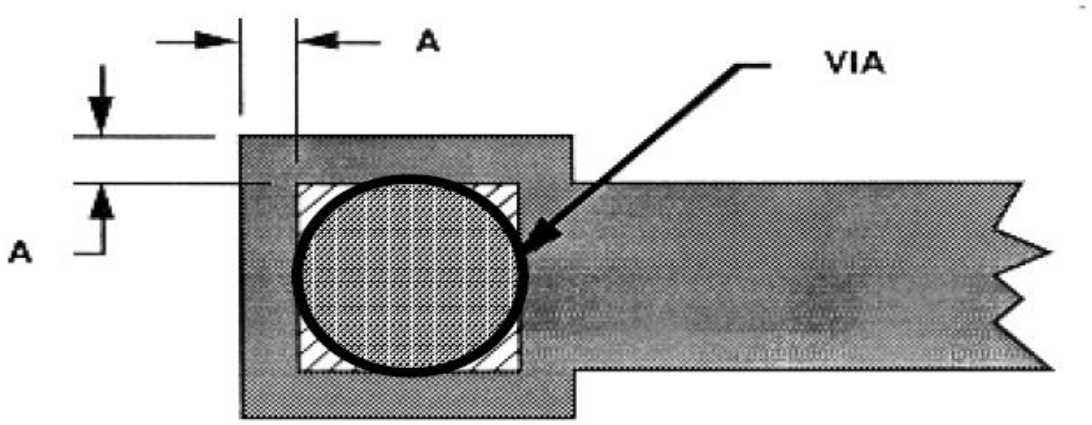
Catch Pads

ELECTRICAL VIAS

Catch Pads

Catch pads above and below each via shall overlap the via on all four sides by a specified distance (see table below). Exception is areas of dense routing that do not permit the use of catch pads over vias (conductor lines terminated directly to vias*).

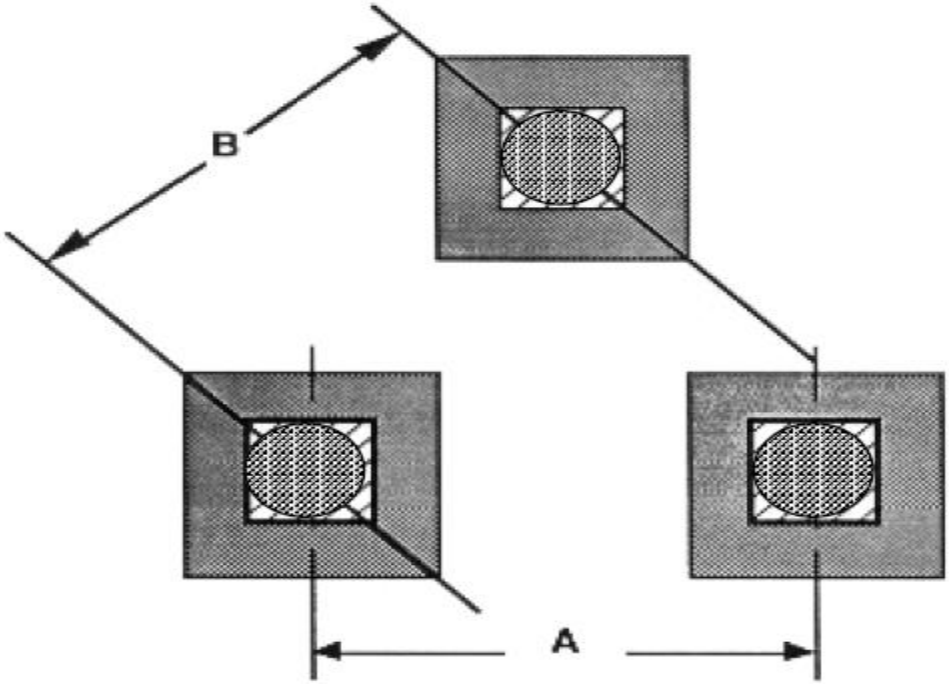
Catch pads may be excluded from RF transition vias.



A = 1 mil minimum

Electrical Vias Rules

Electrical via to via spacing on the same layer



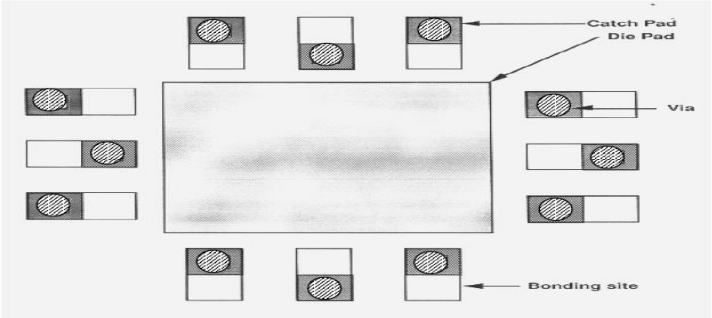
A (min.)	B (min.)
2.0 x via size	2.0 x via size

Design Rules

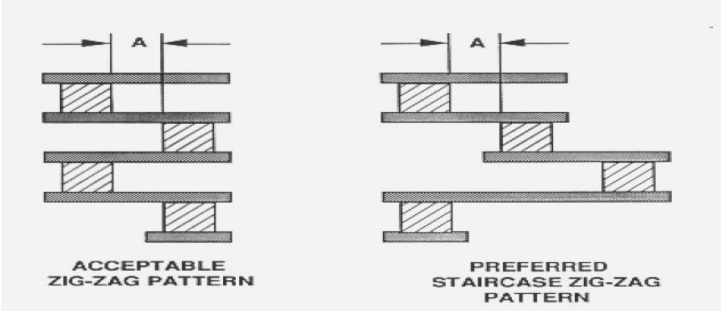
Electrical Vias

Electrical Vias

Where design density necessitates long strings of vias, the vias should be staggered to prevent snapstrate type cracking. The diagram below is an example of an staggered via pattern.



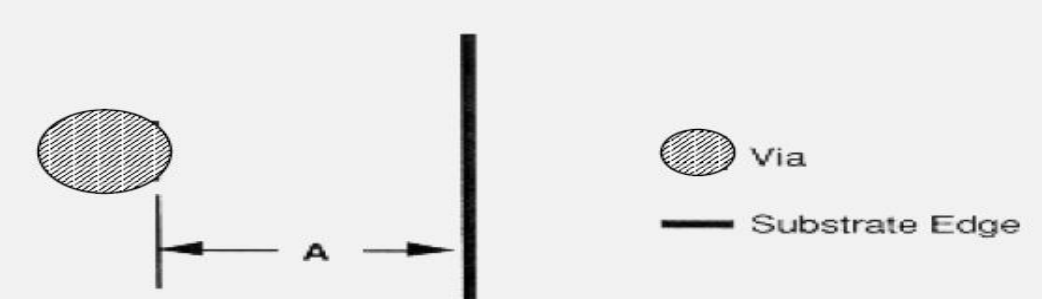
Electrical via to electrical via stagger for layer to layer connections. Vias may stagger (zig-zag) vertically to minimize blockage of routing channels and reduce via "posting" effects. The diagram below is an example of acceptable via staggering techniques.



A = 0 to 1 via diameter

Electrical Vias

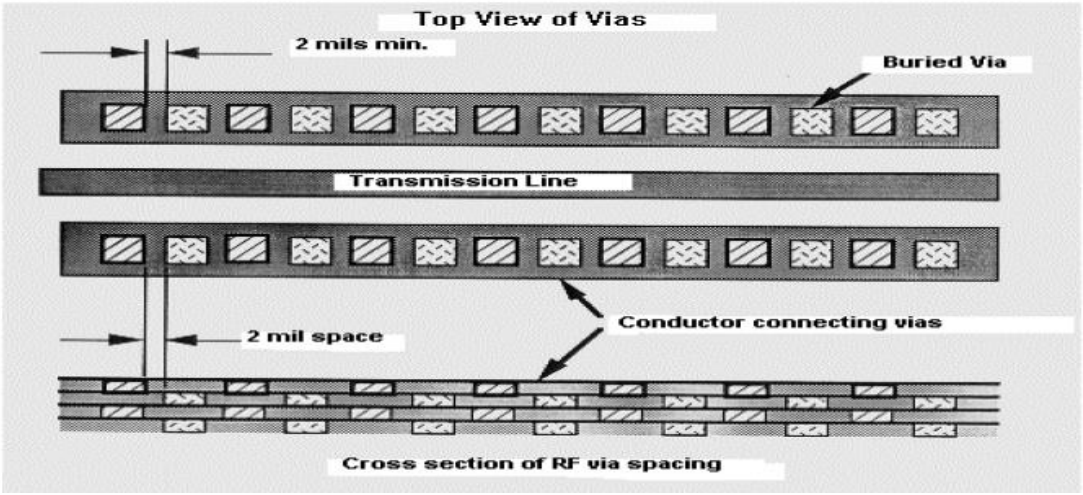
Electrical via to edge of substrate



A= 2 Via Diameters

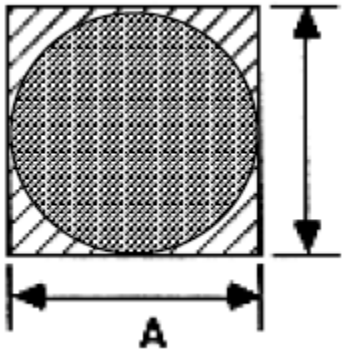
RF Vias

Designs Requiring high frequency line and controlled impedance lines may require buried coaxial type shielding which is accomplished by placing vias parallel to the controlled lines through out the shielded cross sectional area. RF vias may be paced as close as 2 mils apart (horizontal displacement on adjacent layers) as long as they are electrically common to each other. RF vias may also be stacked if required as long as they maintain 2 via diameters pitch minimum. See diagram below.



Via Design Rules

Thermal Vias

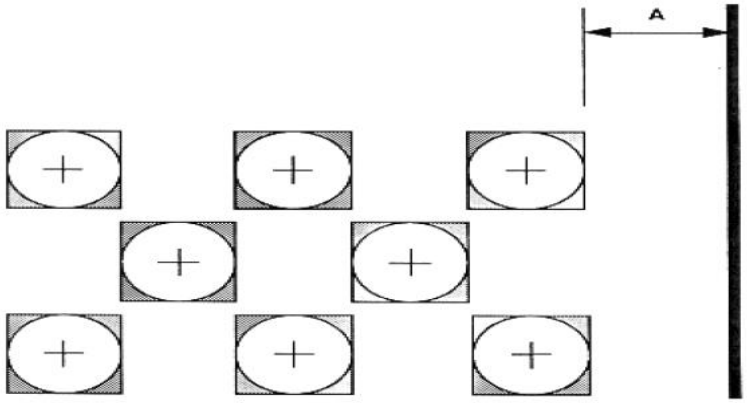


A = 4,6,8,10,12,16, MILS

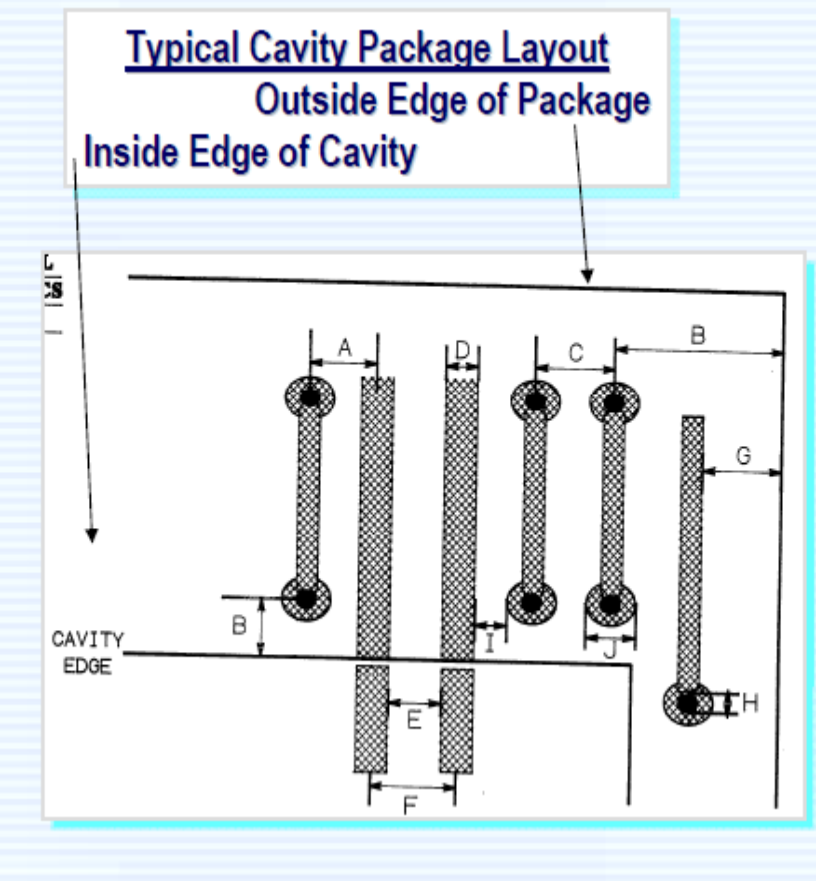
The maximum thermal via array size using the 6 mil hexagonal or 10 mil rectangular size is 250 mil. Length or width. Larger thermal arrays using layer via diameters with 3 x via diameter spacing are available upon request.

Thermal via to edge of substrate clearance

A = 60 MILS



Design Layout Rules

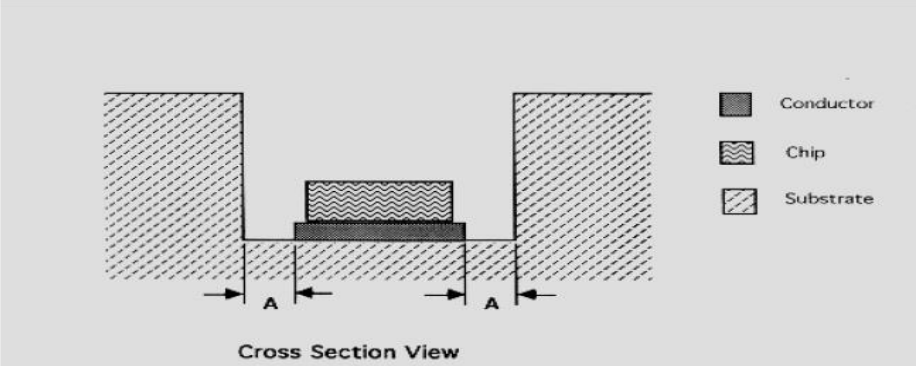


	Features	Layout Spacing (inches)
A	Via to trace pitch	0.008 (min)
B	Via to cavity edge	0.005 (min)
	RF ground to cavity edge	0.003
	RF line to cavity edge	0.0015
C	Via to via pitch	2 X via size
D	Line Width	0.004 (0.003 in small area)
E	Line to Line Spacing	0.004 (.003 in small area)
F	Line to Line Pitch	0.006 min
G	Line to edge	0.005
H	Via Diameter	0.004 min
I	Line to cover pad	0.003

Design Layout Rules

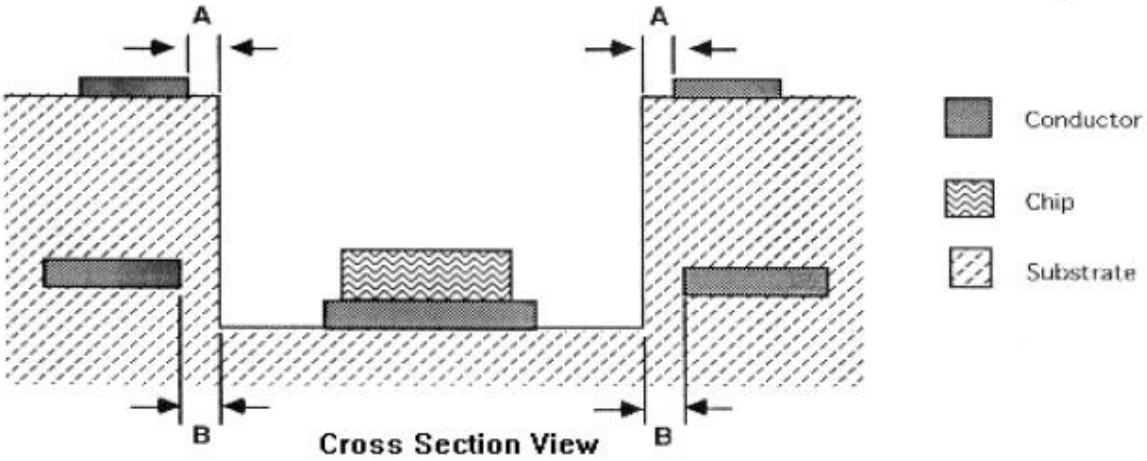
Cavities

Cavity bottom conductor to cavity wall clearance



A = 2.5 mils min

Exposed/buried conductor to cavity wall clearance



A Exposed	**5 mils**
B Buried	5 mils

Metals, and Braze Alloys

for Seal Rings, Heat Sinks, and Lead Frames

Joint	Metal	Braze Alloy	Comments
Heat sink to ceramics	Cu-Mo Cu-Mo-Cu Al-Si-C Cu, 99% Mo	72Ag-28Cu (Cusil) (779 °C)	For substrates less than 3 inches in length and diameter
Heat sink to ceramics	Cu-Mo Cu-Mo-Cu Al-Si-C Cu, 99% Mo	80Au-20Sn (280 °C) 88Au-12Ge (356 °C)	For substrates more than 3 inches in length and diameter
Seal ring to ceramics	Kovar	72Ag-28Cu (Cusil) (779 °C)	For substrates less than 3 inches in length and diameter
Seal ring to ceramics	Kovar	80Au-20Sn (280 °C) 88Au-12Ge (356 °C)	For substrates more than 3 inches in length and diameter

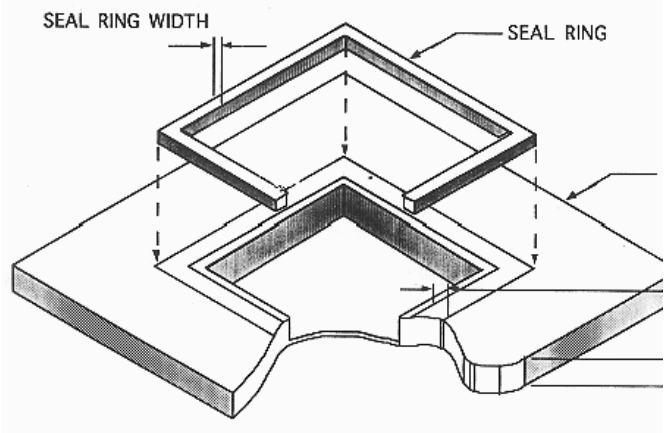
Soldering/Brazing – Thermal Matching

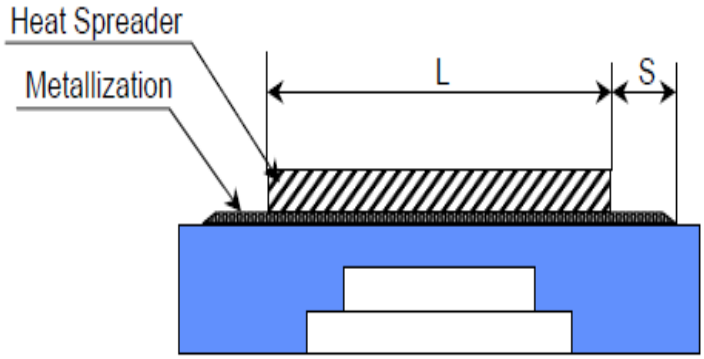
Available Solder Alloys for HTCC

Solder Alloy	Reflow Temperature
72Ag-28Cu	779 °C
88Au-12Ge	345 °C
80Au-20Sn	280 °C
88Pb-10Sn-Sag	267-299 °C
96Sn-4Ag	221 °C
63Sn-37Pb or 62Sn-36Pb-2Ag	179 °C

Brazing / Soldering Design Consideration

Brazing / Soldering of Seal Rings, Heat Sinks, Edge Connectors etc. – a Standard Practice in HTCC Technology.





- Metal seal ring cross section should be 30 mils minimum. Ring frame corners should be radiused.
- Kovar leads and rings should be fully annealed prior to plating.
- Metal lead cross section and width should be minimized to reduce stress at the attachment site.
- Metal seal rings and leads should be plated with Ni and then Au.
- Metal seal ring aspect ratio height / width should not exceed 2.
- Preparatory metallization width should be, as minimum, 40 mils wider than seal ring, 80 mil is preferred. Top barrier metal should overlap bottom adhesion metal 5 mils/side. Metallization corners should be radiused to prevent solder pooling and reduce stress risers.
- Provide for dielectric solder dam material around solder sites. Dielectric should overlap barrier metal 2-5 mils/side.
- Lead or pin attachment sites should be 2x the width/diameter of the lead/pin.

Plating Options

Following Plating finishes are available for all exposed metalized surfaces

Plating Options	Comment
Electrolytic Gold	Plating thickness from 10 µ" to > 50 µ"
Electroless Gold	Plating thickness from 10 µ" to > 50 µ"
Electrolytic Nickel	Plating thickness > 100 µ"
Electroless Nickel	Plating thickness > 100 µ" with Au flash

Contact Us

Thank you for considering NEO Tech your AlN package and interconnect requirements.

We can be reached at.....

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