

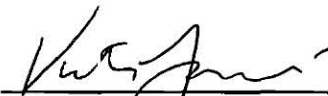
# PCB Fabrication Specification

Rev	Change Description	Changed By	Release Date	Effective Date
A	Initial Release	S. Babiuch	8/25/2016	8/29/2016
B	Changes throughout	S. Babiuch	9/9/2016	9/9/2016


**Approvals:**

  
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9/9/16  
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9/9/2016  
 Date

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## 1.0 Purpose

This specification establishes the NEO Tech fabrication requirements for printed circuit boards.

The order of precedence for documentation detailing fabrication requirements shall be as follows:

- 1.1 NEO Tech Purchase Order - any specific notes printed on the PO.
- 1.2 Customer Fab drawing (including array drawings if applicable), Master Artwork and/or Gerber Files  
This includes fab and/or array drawings generated by NEO Tech for internal use. It also includes customer or NEO Tech approved specific issues regarding the data, manufacturing or design of the Part Number documented from a SELLER DFM, EQ or other design review process prior to fabrication.
- 1.3 Customer Specification (if applicable)
- 1.4 NEO Tech PCB Fabrication Specification (this document).

## 2.0 Scope

This specification applies to all PCBs (Printed Circuit Boards) procured by NEO Tech for all facilities.

## 3.0 Definitions

- 3.1 **U.L.** .....Underwriter's Laboratories, Inc.
- 3.2 **BUYER** .....NEO Tech
- 3.3 **SELLER** .....Purchase Order recipient, Supplier, PCB Fabricator
- 3.4 **Customer** .....NEO Tech's Customer
- 3.5 **EQ (Engineering Query), TQ (Technical Query), DFM (Design for Manufacturability)**  
An evaluation of the fab drawings and Gerber data done by the SELLER and sent to the buyer to request design and/or data deviations, clarity or exemptions.
- 3.6 **PO** .....Purchase Order
- 3.7 **PCB** .....Printed Circuit Board
- 3.8 **P/N** .....Part Number


#### 4.0 Reference Documents

- 4.1 IPC-6012..... Qualification and Performance Spec for Rigid Printed Circuit Boards-and all IPC Applicable Documents referenced therein.
- 4.2 IPC-6013..... Qualification and Performance Spec for Rigid-Flex and Flex Printed Circuit Boards
- 4.3 UL STD 94 ..... Tests for Flammability of Plastic Materials for Parts in Devices and Appliances

**NOTE:** All Standards or Test methods in this document are referenced in the above documents.

#### 5.0 Roles and Responsibilities

Role	Responsibilities
<b>SELLER (Supplier)</b>	<ol style="list-style-type: none"> <li>1. This document is referenced on all BUYER purchase orders for PCBs through the Quality Clauses. The SELLER shall follow the order of precedence noted above for fabrication and delivery of PCBs.</li> <li>2. SELLER shall inform BUYER if there are any discrepancies between the BUYER purchase order, BUYER customer information and the BUYER specifications.</li> <li>3. SELLER shall obtain and review all Customer Specifications referenced on the fabrication drawings.</li> <li>4. Design documentation provided by BUYER shall be considered proprietary information and shall not be disclosed to third parties without prior written permission.</li> </ol>
<b>BUYER (NEO Tech)</b>	<ol style="list-style-type: none"> <li>1. Corporate PCB Commodity Management shall maintain this document and assure that the BUYER website has the latest revision.</li> </ol>

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## 6.0 Procedure

### The SELLER shall meet the following FABRICATION SPECIFICATIONS

Unless designated by BUYER on the Purchase Order (Section 1.1 above), all products are to be built to the following minimum standards: customer specifications and documentation (1.2 and 1.3 above), or IPC 6012 Class 2 (latest revision), whichever is more stringent, and the requirements in Section 6 below. Any deviations to this specification, without written approval from BUYER, are strictly prohibited. Exceptions to this specification must be obtained in writing from BUYER on an individual part number basis.

6.1 Flex and Rigid-Flex PWB's shall be fabricated to meet IPC-6013, Qualification and Performance Specification, Class 2 requirements and the requirements in Section 6 below.


### 6.2 Artwork and Fabrication Drawing Requirements

- 6.2.1 FABRICATION DATA for a first time purchase or new revision, BUYER shall provide to SELLER the most recent customer fabrication data which shall include at minimum Gerber files. If the customer data includes both ODB++ and Gerber data, and SELLER chooses to use the ODB++ data for fabrication, SELLER must compare the two data files. If there are discrepancies between the data files, it must be reported to BUYER and approval obtained before using the ODB++ data for fabrication. At no time shall SELLER use ODB++ format data for fabrication without comparing to Gerber format data.
- 6.2.2 Other than allowances for produce-ability, there shall be no modifications of the master artwork or Gerber data, or change in material specifications, without prior authorization from BUYER Engineering. All deviations to the fabrication drawing(s) or array drawing(s) must be approved by BUYER.
- 6.2.3 The SELLER is responsible for verifying that master artwork and/or Gerber data revision levels are in accordance with the master drawings and BUYER purchase order. If there are any discrepancies, BUYER shall be notified for resolution.
- 6.2.4 The fiducial diameter on the finished PCB must be within  $\pm 0.002$  of the original artwork/Gerber data. All fiducials are to be **FLASHED** for plotting purposes.
- 6.2.5 All SELLER design reviews (or EQs) on new PNs shall contain the stack-up for that P/N. At a minimum, a stack-up shall show copper weights and thicknesses, material types, di-electric thicknesses, plies and types of pre-pregs used.

### 6.3 Array Requirements

**BUYER will always purchase quantities per an individual board basis, not arrays.**

- 6.3.1 All boards fabricated in a multiple up array must be individually numbered, either in copper or silkscreen on the top side of the board.
- 6.3.2 X-outs (rejected pieces) within the array are not permitted unless indicated on BUYER purchase order, BUYER array drawing, or with written authorization from BUYER engineering prior to shipment.
- 6.3.3 When X-outs boards are permitted, the following shall apply:

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- 6.4.1.1 X-out boards must be identified by using a permanent black wide tip marker on both sides of the PCB or other identification method agreed to with BUYER engineering (in writing). The marking method used must withstand the entire assembly process and remain identifiable throughout the assembly process.
- 6.4.1.2 All X-outs boards must be packaged and labeled separately from the acceptable product. The maximum # of X-outs per array is 10% or 1, whichever is greater. The maximum amount of X-out arrays per shipment is 10%.

#### **6.4 Machining Requirements**

- 6.4.1 Unless otherwise noted, tolerance .xx ± 0.01", .xxx ± 0.005".
- 6.4.2 SMT Feature Accuracy: Feature to Feature location tolerance +/-76um (0.003").
- 6.4.3 Board tooling hole locations to be ± 0.003" repeatable from board to board for automatic insertion. These tooling holes must be drilled with the same program as the component holes. Tooling holes shall not be plated.

#### **Edge Connector Requirements**


- 6.4.4 Unless otherwise specified on the customer or BUYER drawings, the following shall apply:
  - 6.4.1.3 All plug-in edge connectors must be chamfered or beveled.
  - 6.4.1.4 Unless otherwise specified, the angle of the chamfer shall be 45°, with a depth of 0.020" ± .010".
  - 6.4.1.5 A chamfered edge shall have no separation of plating on printed contacts and no loose glass fibers on the beveled edge.
  - 6.4.1.6 Unless otherwise specified, keying slots shall be centralized between printed connector contacts within BUYER's fabrication drawing tolerance.

#### **6.5 Plating Requirements**

- 6.5.1 All plating requirements to meet IPC-6012 Class 2 (most current revision).
- 6.5.2 Plating thieving patterns are allowed within the borders of the BUYER array rails or frames, provided the plated area is copper and then covered with solder mask material. Plating thieving patterns shall be a minimum 0.200" from any fiducial or feature on the array. There shall be no plating thieving patterns within the area of the final piece without BUYER customer approval.

#### **6.6 Solder Mask Requirements**

- 6.6.1 Solder masking must meet the acceptability requirements of IPC-SM-840 (Class 2) and IPC-A-600 (latest revisions) and be of the type specified on customer documentation. There shall be no solder mask on plated hole pads within the minimum annular ring requirements. There shall be no soldermask on SMT pads.
- 6.6.2 Via Plugging height- Shall be no greater than 0.003" above via pad.

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## 6.7 Silkscreen Requirements

6.7.1 Silkscreen inks shall be non-conductive and of the color specified on customer documentation unless otherwise noted. Silkscreen patterns and silkscreen ink shall maintain the same clearances from solderable features as soldermask.

## 6.8 Testing Requirements

6.8.1 SELLERs of PCBs shall perform Net List testing on 100% of the boards per IPC Specification 9252 (latest revision). Mark each board image to signify passing electrical tests. Welding traces is not allowed without approval from the customer.

### 6.8.2 Impedance Testing Requirements

If an impedance requirement is identified on the drawing / specification, SELLER of the PCB shall perform appropriate impedance testing of either PCBs or impedance coupons fabricated on the same working panels as the PCBs for each date code shipped to the purchase order and shall include a statement of Impedance Conformance in the Certificate of Conformance (C of C). Impedance coupons shall be traceable to the date code shipped. SELLER shall maintain records of test results per date code per the Document / Data Retention quality clause. Any deviation from this requirement shall be approved in writing by BUYER Quality Engineering before shipment.

## 6.9 SELLER Markings/Samples

6.9.1 At minimum, SELLER to permanently date code (week, year) each board/array and provide SELLER identification and U.L. code designation on each individual board that will remain legible through wave soldering and cleaning processes.


6.9.2 SELLER to provide a sample PCB for solder testing with each date code of parts shipped. Sample piece may be a scrap board (for a non-solderability related defect).

## 6.10 Outdated PCB Requirements

6.10.1 A shipment of **OSP, Immersion Silver, Immersion Tin** finish boards more than **three months** old (per date code) will be accepted with prior written BUYER approval and submittal of solderability test data with the shipment.

6.10.2 A shipment of **Hot Air Solder** (HASL) finish boards more than **six months** old (per date code) will be accepted with prior written BUYER approval and submittal of solderability test data with the shipment.

6.10.3 A shipment of **Gold** (ENIG) finish boards more than **six months** old (per date code) will be accepted with prior written BUYER approval and submittal of solderability test data with the shipment.

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## 6.11 Packaging Requirements

- 6.11.1 Shipping boxes not to exceed 35 pounds.
- 6.11.2 Shipping carton to be marked with SELLER name, date codes, vendor lot number, purchase order number, quantity in the carton, part number and revision number or per Bar Code Standards requested. If more than one date code is to be shipped in a box, they must be clearly identified on the packages.
- 6.11.3 The packaging shall be done in a way to prevent damage to the product edges / corners using industry acceptable methods and must include (ref Reference IPC Spec 1601:2010 Section 4):

*Vacuum Sealed Moisture Barrier Bag (MBB)*

*Humidity Indicator Card (HIC)*

*Desiccant compatible with PCB and finish*

*Slip sheets between each PCB (optional)*

*Suitable bubble wrap if needed to protect PCB inside MBB*

- 6.11.4 Solderability samples and cross section samples should be packaged separately at the top of the box.
- 6.11.5 All silver finish PCBs must be packed with silver saver paper in between each PCB.
- 6.11.6 Shelf Life Requirements

When stored in a controlled environment and in the original packaging, surface finish shelf life requirements based on receipt at BUYER facility:


*6 months ..... OSP, Immersion Silver, Immersion Tin*

*12 months .... HASL*

*12 months .... ENIG*

## 6.12 Quality Requirements

- 6.12.1 Boards must exhibit a minimum annular ring of 0.001" of copper around component holes. SELLER is responsible to verify that this requirement can be met with the artwork provided.
- 6.12.2 The PCB fabrication process and materials must be recognized by U.L. Processed board material must have a minimum rating of 94V-0 or the highest rating possible based on the laminate material type. SELLER shall provide their U.L. File number on the Certificate of Conformance with each shipment.
- 6.12.3 For cleanliness, PCB's shall be measured after final surface coating application in accordance with IPC-TM-650, Method 2.3.25 paragraph 4, Resistance of Solvent Extract Method. The ionic contaminant level shall not be greater than 6.45 µgm NaCl/in<sup>2</sup>.
- 6.12.4 Boards must meet the solderability requirements when tested in accordance with the J-STD-003 and appropriate Test Methods. Results must be submitted for each date code supplied to BUYER along with the Certificate of Compliance. BUYER reserves the right to reject the entire date code of boards when samples cannot meet this criterion.

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6.12.5 Plating thickness and hole wall integrity shall be verified in the smallest thru via and the smallest blind via per Methods IPC-TM-650 2.1.1 for micro-section preparation and IPC-TM-5.6.8 for thermal stressing (solder float).

#### 6.12.6 PCB Positive Etch-Back Requirements

If positive etch-back is required (applicable to multilayer FR4 / Polyimide PWBs), all vias shall be flush with conductor patterns on external layers and the minimum via wrap requirement shall be maintained. Cross section samples and measurement data correlated to the sample location measured or copies (photos) and measurement data of samples per the applicable IPC/Military specification, as specified on the drawing, shall be provided by the manufacturer with the deliverable product. The sample SHALL be in accordance with the applicable IPC / Military specification and as a minimum representative of the minimum and maximum diameter BLIND, MICRO and THRU vias contained within the subject PWB and clearly exhibit etch-back and via characteristics. It is highly suggested that the micro-section sample(s) be taken from an actual PWB from each panel rather than from the standard IPC/Military panel coupon.

### 6.13 Shipping Deliverables

#### 6.13.1 Certificate of Conformance (C of C)

Certificate of Conformance is required with each shipment and must include:

- (a) a statement that all applicable requirements have been met
- (b) a signature of the person responsible for the quality of the product
- (c) contain the following information as a minimum:
  - Seller Name
  - NEO Tech Part Number and revision
  - NEO Tech Purchase Order #
  - Shipment Quantity
  - Lot Code (work order #)
  - Date Code

All PCB Brokers (Intermediate Organizations), Manufacturers Reps or Agents shall provide the actual manufacturer's name and facility location on the Certificate of Conformance with each shipment to BUYER.

6.13.2 The C of C shall contain any additional information invoked by subsequent Quality Clauses or this specification such as those (but not limited to) examples below:

6.13.2.1 UL File # (per Section 6.9.1)

6.13.2.2 Impedance Test data (per Section 6.8.2)

6.13.2.3 Solderability data (per Section 6.12.4)

6.13.2.4 Cleanliness data (per Section 6.12.3)

6.13.2.5 Electrical Test statement per (Section 6.8.1)

6.13.2.6 Micro-section report including data / results and pictures (per Section 6.12.5)

6.13.2.7 Micro-section potted coupon from report and PCB it was taken from.

6.13.2.8 Positive etch back (if required) verification (per Section 6.12.6)

6.13.2.9 One solder sample PWB from the same date code as the lot.